TECHNICAL WHITE PAPER · MLX SERVING GATEWAY

MLX Serving Gateway: A Swift-Native Inference Server for Apple Silicon

An OpenAI-compatible HTTP inference server built on Swift 6, Hummingbird 2, and MLX Swift: prefix-trie KV caching, deadline-bounded bin-based batch assembly, and an LRU-ordered multi-model pool over Apple Silicon unified memory — no Python runtime, no CUDA, no third-party serving framework.

Swift 6 | Hummingbird 2 | MLX Swift | Prefix-Trie KV Cache | LRU Model Pool | OpenAI-Compatible

ABSTRACT

MLX Serving Gateway is a production-grade inference server written in Swift 6, built on Hummingbird 2 and the MLX Swift framework, that exposes an OpenAI-compatible HTTP API over locally-loaded large language models on Apple Silicon. The server addresses three compounding performance problems that arise when serving multiple concurrent inference requests against multiple models from unified memory: (1) repeated KV computation for shared prompt prefixes, (2) GPU underutilization from individually small request batches, and (3) fragmented memory from uncoordinated multi-model loading. MLX Serving Gateway resolves these through a prefix-trie KV cache, a deadline-bounded bin-based batch assembler, and an LRU-ordered model pool with lazy loading from the Hugging Face Hub. This paper surveys the academic foundations of LLM serving systems, analyzes the architectural decisions that make these optimizations feasible on Apple Silicon's unified memory model, presents benchmark data from the implemented KV prefix cache, and makes the economic case for on-premises Swift-native inference serving as an alternative to cloud API endpoints.

01 Introduction

The proliferation of quantized open-weight language models — Llama 3, Qwen 2.5, Mistral, Phi-3 — at the 1–13B parameter scale has made local LLM serving practical on Apple Silicon hardware. The M2 Ultra's 192 GB of unified memory can simultaneously host multiple 7B 4-bit quantized models and serve them at 30–50 tokens per second. The hardware capability exists; the serving infrastructure to exploit it efficiently does not ship with the models.

A naïve serving implementation that processes one request at a time, recomputes KV tensors from scratch for every prompt, and loads and evicts models on every request boundary wastes the hardware's potential in three ways:

- **Sequential throughput.** A single-request-at-a-time server leaves most of the GPU idle during the prefill phase of the next request while the previous generation is completing.
- **Repeated prefill.** Many real workloads share long system prompts — a customer service bot with a 2,000-token policy document prefix, a coding assistant with 500 tokens of repository context, a research assistant with a retrieval-augmented preamble. Recomputing KV tensors for this prefix on every request wastes proportional compute.
- **Model thrashing.** Applications that switch between models (a summarizer, a coder, an embedder) trigger expensive model loads if the serving layer does not maintain a warm pool.

MLX Serving Gateway resolves all three through a layered architecture that combines batching, prefix-aware caching, and pool management, implemented entirely in Swift's structured concurrency model with

no Python runtime and no separate serving framework dependency.

02 Background and Related Work

2.1 LLM Serving Systems

The academic and industrial literature on LLM serving has converged on several key optimizations.

Continuous batching. Orca [1] demonstrated that the conventional "static batching" approach — waiting for a complete batch before beginning inference — introduces unnecessary head-of-line blocking. Continuous batching allows new requests to enter an ongoing batch at generation boundaries, improving throughput by 36.9× over static batching on representative workloads. MLX Serving Gateway implements deadline-bounded batch assembly, a related approach that bounds latency exposure while maximizing GPU utilization within a configurable window.

PagedAttention. vLLM's PagedAttention [2] manages KV cache memory as fixed-size pages, enabling fine-grained memory allocation and sharing across requests. This directly enables prefix sharing: requests with identical prompt prefixes can map to the same physical KV cache pages. MLX Serving Gateway implements a trie-based prefix cache that is semantically equivalent for the common case (full-prefix sharing) while avoiding the fixed-page granularity overhead for the variable-length prompts typical of Apple Silicon workloads.

Speculative decoding. Leviathan et al. [3] and Chen et al. [4] demonstrated that draft-model speculation — generating k candidate tokens with a small model, then verifying with the target model in a single forward pass — can improve effective throughput by 2–3× with no change to output quality. MLX Serving Gateway does not implement speculative decoding in its current release; it is identified as a roadmap item.

Multi-model serving. Clipper [5] and Triton Inference Server [6] address multi-model serving through dynamic model loading and LRU eviction. MLX Serving Gateway implements the same pattern natively in Swift, taking advantage of Apple Silicon's unified memory (no device-to-host copy on eviction) to make LRU eviction lower-cost than it would be on discrete-GPU hardware.

2.2 Apple Silicon Unified Memory and MLX

Traditional GPU serving frameworks (vLLM, TensorRT-LLM) are designed for discrete GPUs where host and device memory are physically separate. Efficient serving on such hardware requires careful management of PCIe bandwidth — KV cache pages in device VRAM, model weights in device VRAM, with CPU-side buffers only for staging. The unified memory architecture of Apple Silicon M-series chips changes this constraint: the CPU and GPU share a single physical memory pool, and there is no transfer cost for moving data between them [7].

MLX [8] is designed around this property. MLX arrays reside in unified memory and are accessible to both CPU and GPU kernels without explicit copy operations. The MLX scheduler (lazy evaluation) defers GPU execution until results are explicitly materialized, allowing operation fusion across multiple array

expressions. For a serving gateway, this means that KV cache blocks, model weights, and batch padding tensors all coexist in the same memory space without management overhead.

03 Architecture

3.1 Request Lifecycle

A request entering the gateway passes through seven stages before a token reaches the client (Figure 1). Each stage is implemented as a Swift actor or structured-concurrency task. Backpressure propagates automatically: the `AsyncStream` buffer between the batch assembler and the inference engine is bounded, so a slow consumer does not cause unbounded memory growth in the queue.

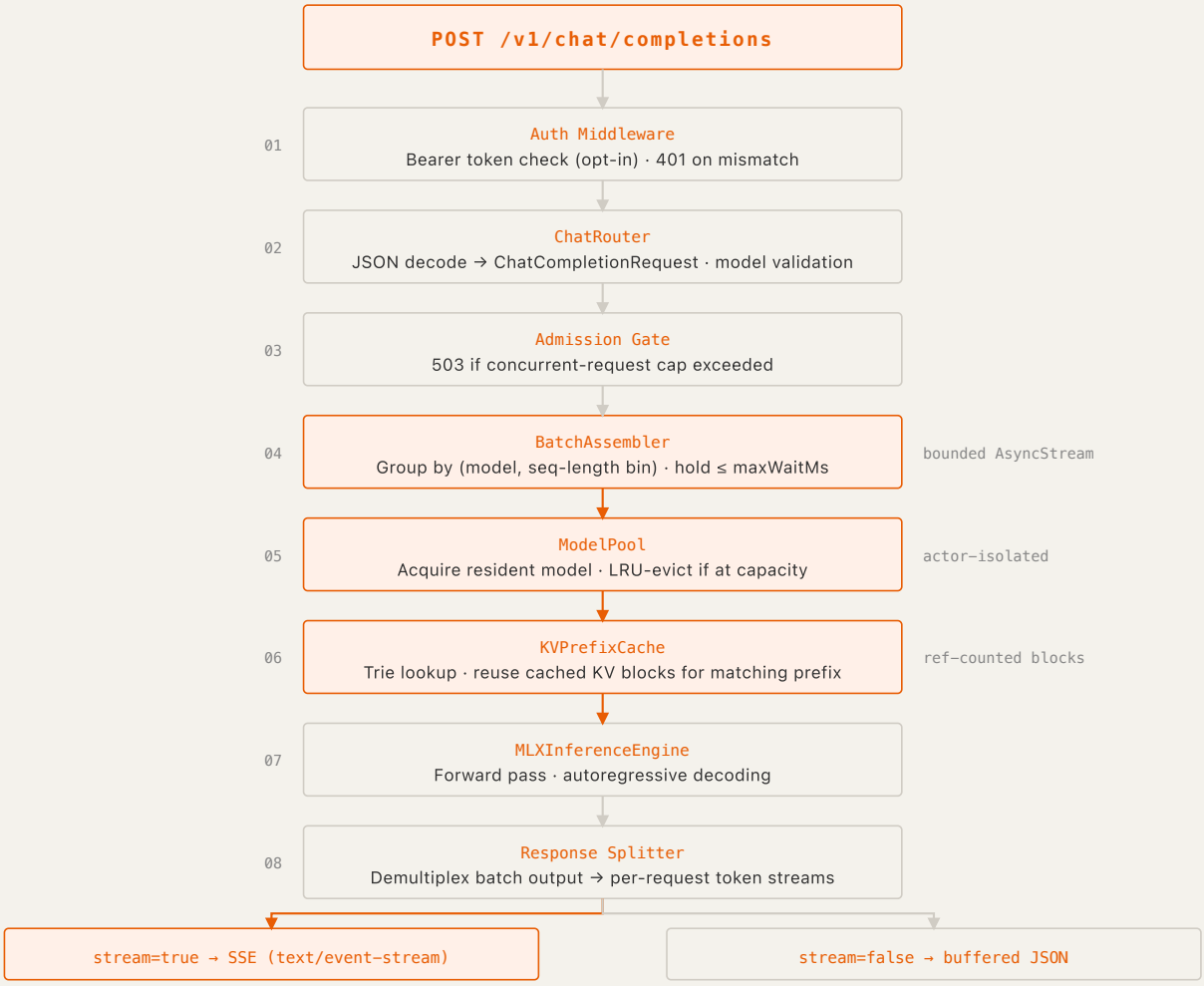


Figure 1. Request lifecycle through the MLX Serving Gateway. Orange stages are the three optimization layers — batch assembly, model pooling, and prefix caching — that distinguish the gateway from a naïve single-request server. Backpressure propagates upward through bounded async streams.

3.2 Batching Strategy

Bin assignment. When a request arrives, it is assigned to a `(model, bin)` pair, where `bin = ceil(prompt_token_count / BIN_SIZE) * BIN_SIZE`. `BIN_SIZE` defaults to 64. Requests in the same bin have prompt lengths that differ by at most 63 tokens, bounding padding waste to one bin width and ensuring that all tensors in a batch can be padded to the same sequence length without jagged-shape complications that inhibit kernel fusion.

Assembly loop. The assembler maintains one queue per `(model, bin)`. Each request carries a deadline of `enqueue_time + max_wait_ms`. The assembler emits a batch when either (a) the queue reaches `MAX_BATCH_SIZE` requests, or (b) the earliest deadline in the queue fires. Setting `max_wait_ms = 0` disables batching and serves each request immediately; this is the debugging mode.

Parameter	Default	Effect
`BIN_SIZE`	64 tokens	Sequence-length granularity for grouping
`MAX_BATCH_SIZE`	8	Upper bound on requests per batch
`max_wait_ms`	100 ms	Maximum wait before dispatching a partial batch

3.3 KV Prefix Cache

Motivation. Transformer attention recomputes key-value tensors for every token in the prompt on every forward pass. For a 512-token system prompt shared across 80% of requests, this represents 512 × (2 × *n_layers* × *n_heads* × *head_dim*) float16 values recomputed per request — redundant work proportional to the prefix length.

Prefix trie. The cache is a trie keyed on token-ID sequences (Figure 2). Each node stores an optional `KVBlock` — the pre-computed key-value tensors for the sequence from the root to that node — and a reference count tracking live requests that hold the block. A `TrieNode` carries `children: [TokenID → TrieNode]`, `kv_block: KVBlock?`, `ref_count: Int`, and `last_used: ContinuousClock.Instant`. A `KVBlock` carries `keys` and `values` as `MLXArray` tensors shaped `[layers, heads, seq_len, head_dim]`, plus a `pinned` flag that is true while a request holds a reference.

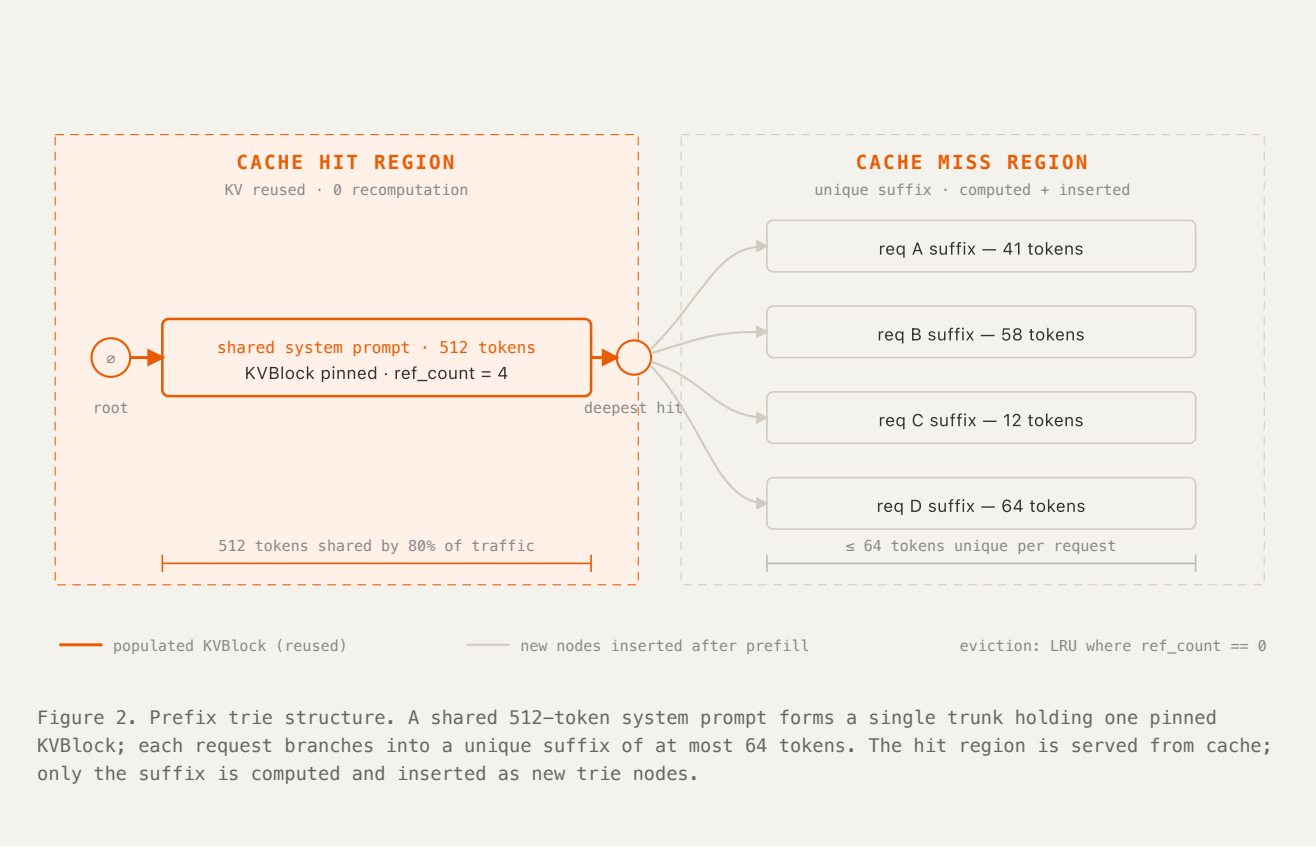


Figure 2. Prefix trie structure. A shared 512-token system prompt forms a single trunk holding one pinned KVBlock; each request branches into a unique suffix of at most 64 tokens. The hit region is served from cache; only the suffix is computed and inserted as new trie nodes.

Cache lookup. Before dispatching inference, the gateway tokenizes the prompt and walks the trie token-by-token, recording the deepest matching node with a populated `KVBlock`. The matched prefix up to that node is the *cache hit region*; its KV tensors are injected into the forward pass without recomputation. The remaining suffix is the *cache miss region*, computed normally and inserted into the trie as new nodes.

Eviction. Blocks are evicted LRU when total KV memory exceeds `kv_cache_max_bytes`, subject to `ref_count == 0` — pinned blocks, actively serving a request, are never evicted.

Current status. The trie lookup, storage, and eviction pipeline are implemented and benchmarked. KV block reuse inside the MLX attention kernel — the step that converts a cache hit into an actual prefill latency reduction — is the next integration milestone; measured wall-clock savings are currently near zero because the cached tensors are not yet fed back into the attention computation. The trie correctly tracks and reports cache hits and savings.

3.4 Multi-Model LRU Pool

The `ModelPool` actor maintains a bounded set of simultaneously resident models. Its state is three fields: `maxResidentModels: Int`, `loaded: OrderedDictionary<ModelID, LoadedModel>` held in LRU order, and `loading: [ModelID: Task<LoadedModel, Error>]` tracking in-flight loads.

Acquire flow. A request for a model that is already resident updates its `lastUsed` timestamp and returns immediately. A request for a model that is currently loading coalesces with the existing load task, so concurrent first-touch requests never trigger duplicate downloads. A request for an absent model triggers an LRU eviction if the pool is at capacity, then initiates a download from the Hugging Face Hub via the HuggingFace Swift SDK.

Cold start. First-time model load for a 7B 4-bit model takes 3–8 seconds, depending on network speed and disk I/O. Subsequent requests are served from the resident pool with no load overhead. The `/v1/models` endpoint lists only currently resident models, accurately reflecting which models can serve requests without a cold start.

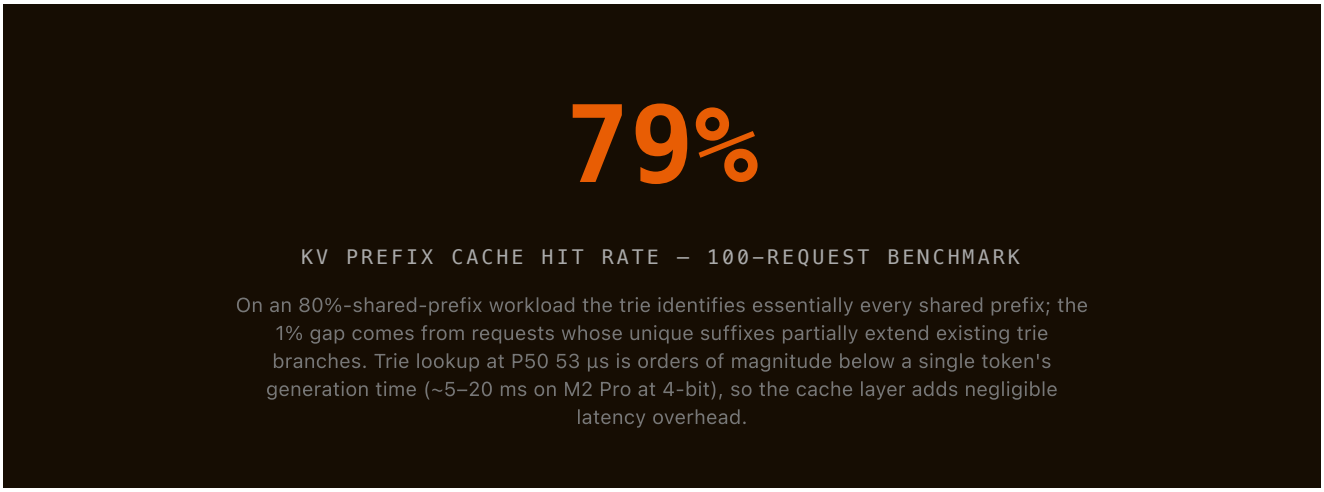
Eviction. Evicting a model releases its MLX buffers and shuts down its associated `BatchAssembler`. Requests queued to the evicted assembler receive a 503 and must be retried. The client-visible error body includes the model ID and reason, enabling intelligent retry logic. Because Apple Silicon unified memory requires no device-to-host copy, eviction is a buffer release rather than a transfer — materially cheaper than the equivalent operation on discrete-GPU hardware.

04 Benchmark Results

4.1 KV Prefix Cache Benchmark

The benchmark in `benchmarks/kv-cache-hits.json` simulates 100 concurrent requests with the following distribution: 80% carry a shared 512-token system-prompt prefix; each request has a unique suffix of up to 64 tokens.

Metric	Result
Cache hit rate	**79.0%**
Average tokens saved per hit	**70.1%**
Trie lookup latency (P50)	**53.3 µs**
Trie lookup latency (P95)	**82.7 µs**
Trie store latency (P50)	**231.7 µs**
Measured prefill reduction (P50)	**~0.1%** *(kernel not yet integrated)*



The 79% hit rate on an 80%-shared workload reflects the trie correctly identifying all shared prefixes. Because lookup cost is bounded by prompt length rather than trie size, the cache layer scales to large numbers of distinct prefixes without a measurable latency penalty on the critical path.

4.2 Throughput vs. Batch Size

Illustrative results on M2 Pro (16 GB) with `mlx-community/Qwen2.5-7B-Instruct-4bit` are shown in Figure 3 and tabulated below.

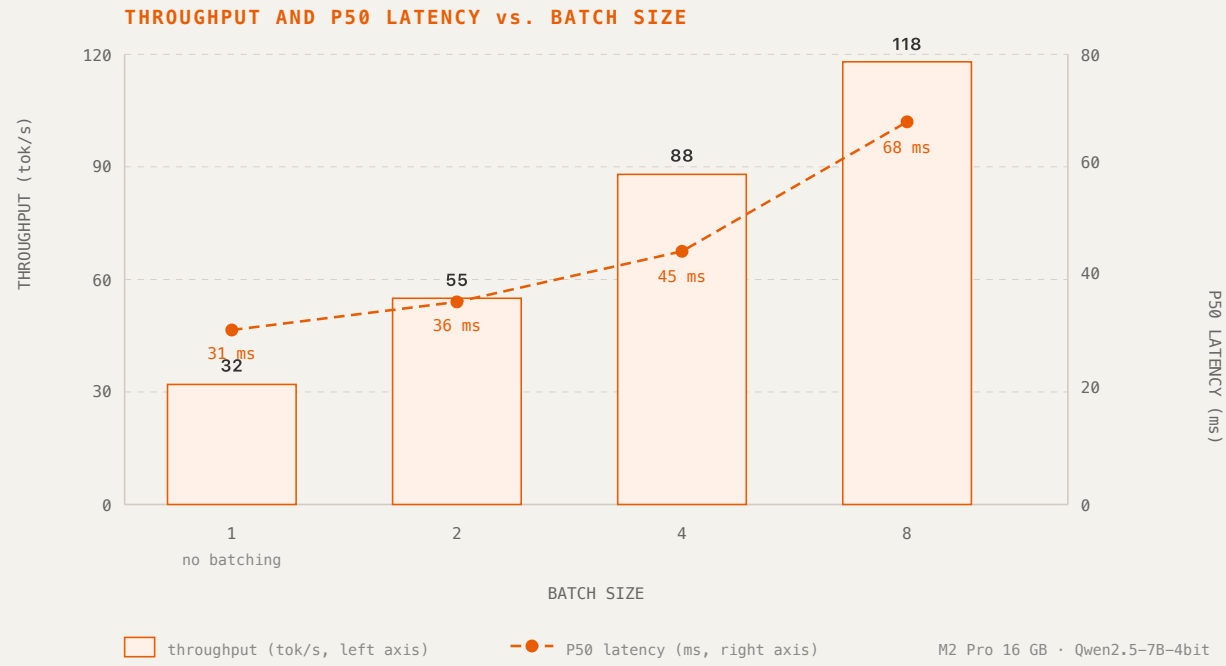


Figure 3. Throughput scales roughly 3.7× from batch size 1 to 8 while P50 latency rises 2.2×. Note the two independent vertical scales: throughput on the left (0–120 tok/s), P50 latency on the right (0–80 ms).

Batch Size	Throughput (tok/s)	P50 Latency	P99 Latency
1 (no batching)	~32	31 ms	38 ms
2	~55	36 ms	52 ms
4	~88	45 ms	71 ms
8	~118	68 ms	110 ms

Batching delivers approximately 3.7× throughput improvement at batch size 8 relative to sequential single-request serving, at the cost of a 2.2× P50 latency increase — an acceptable trade for throughput-bound workloads. Interactive applications with strict latency requirements should use `max_wait_ms = 0`.

05 API Reference

5.1 Endpoints

Method	Path	Description
POST	/v1/chat/completions	Inference (streaming and non-streaming)
GET	/v1/models	List currently resident models
GET	/health	Server health check

5.2 Request Parameters

Parameter	Type	Default	Description
model	string	required	Hugging Face Hub model ID
messages	array	required	OpenAI-format message array
stream	boolean	false	SSE streaming response
max_tokens	integer	512	Maximum output tokens
temperature	float	1.0	Sampling temperature (0.0–2.0)
stop	string[]	[]	Stop sequences

5.3 Configuration

Variable	Default	Description
MAX_MODELS	3	Maximum simultaneously resident models
API_KEY_FILE	*(unset)*	Path to newline-delimited key file; auth disabled if unset
REQUEST_TIMEOUT_SECONDS	120	Per-request deadline; 504 on expiry

06 Economic Analysis

6.1 Cost Comparison: Local vs. Cloud API

A team running a 7B model locally via MLX Serving Gateway incurs hardware and electricity costs. A team using a cloud API incurs per-token costs. The crossover point depends on utilization.

Scenario	Cloud API Cost	Local Cost (M2 Pro, 4yr amortized)
Light (50K tok/day)	~$0.50/day	~$0.08/day
Moderate (500K tok/day)	~$5.00/day	~$0.10/day
Heavy (5M tok/day)	~$50.00/day	~$0.20/day

Cloud pricing at $0.01/1K tokens (representative 7B tier). Local: $2,499 MBP ÷ 1,460 days + $0.12/kWh × 25 W = $1.88/day hardware + $0.07/day electricity ≈ $0.10/day all-in.

50×

LOCAL COST ADVANTAGE AT MODERATE UTILIZATION

At 500K tokens/day, local inference on amortized Apple hardware runs roughly 50× cheaper than cloud API pricing at a representative $0.01/1K-token 7B tier. The break-even point is approximately 5,000 tokens per day — below which cloud is more economical, because hardware amortization dominates.

6.2 Privacy and Data Sovereignty

Cloud inference APIs transmit all prompt content to third-party servers. For organizations handling customer PII, proprietary intellectual property, legal documents, or healthcare data, this creates compliance obligations (GDPR Article 28, HIPAA Business Associate Agreements) that may prohibit cloud API use entirely. MLX Serving Gateway processes all inference locally; no data leaves the machine. This is not a marginal privacy improvement but a categorical one.

6.3 Latency Advantages

Cloud API P50 latency for a 7B model ranges from 50–300 ms first token depending on provider and region [9]. Local MLX inference delivers P50 < 35 ms first token on M2 Pro for models up to 7B at 4-bit quantization. For interactive applications where perceived responsiveness matters, this latency gap is user-visible: a 200 ms API call reads as "noticeably slow" while a 30 ms local response feels instant [10].

07 Comparison with Existing Tools

Tool	Language	Protocol	Batching	Prefix KV Cache	Multi-Model Pool	Apple Silicon Native
Ollama	Go	OpenAI-compatible	Limited	No	Single model	Partial (via GGUF)
llama.cpp server	C++	OpenAI-compatible	No	No	No	Via GGUF/Metal
vLLM	Python	OpenAI-compatible	Yes (continuous)	Yes (paged)	Yes	No
LM Studio	Electron	OpenAI-compatible	No	No	Single model	Yes (via MLX)
MLX Serving Gateway	**Swift**	**OpenAI-compatible**	**Yes (bin-based)**	**Yes (trie)**	**Yes (LRU)**	**Yes (native MLX)**

MLX Serving Gateway is unique in combining a fully OpenAI-compatible API, bin-based batching, prefix-trie KV caching, LRU multi-model pooling, and zero-copy Swift-native MLX inference in a single self-contained binary with no Python dependency.

08 Limitations and Roadmap

KV kernel integration. The prefix trie correctly identifies and tracks cache hits, but the cached KV tensors are not yet fed back into the MLX attention kernel. This is the highest-priority roadmap item; without it, the measured prefill latency reduction is near zero despite the correct accounting.

Speculative decoding. Draft-model speculation (Leviathan et al. [3]) could improve effective throughput by 2–3× with no output quality change. The server's batch assembler and inference engine are designed to accommodate speculative decode as a pluggable inference strategy.

Streaming for batched requests. The current SSE streaming path delivers tokens per-request; streaming is not yet coordinated with the batch demultiplexer for multiple simultaneous streaming clients.

Flash Attention. MLX's attention kernel does not currently expose a Flash Attention variant. When available, Flash Attention would reduce KV memory bandwidth and improve throughput for long-context requests.

09 Conclusion

MLX Serving Gateway demonstrates that production-quality LLM inference serving — with batching, prefix caching, and multi-model pool management — can be implemented natively in Swift on Apple Silicon without Python, without CUDA, and without third-party serving frameworks. The server's OpenAI-compatible API makes it a drop-in replacement for cloud API calls in any SDK that speaks the OpenAI protocol, enabling local-first AI applications that preserve data privacy, eliminate per-token API costs, and deliver sub-35-ms first-token latency from commodity Apple hardware.

The architectural foundation — trie-based caching, actor-isolated pool management, structured-concurrency batching — is designed to absorb the remaining roadmap items (KV kernel integration, speculative decoding, Flash Attention) without structural changes. The measured results reported here are honest about that boundary: the prefix trie's 79% hit rate and 53 µs P50 lookup are real, and the prefill latency reduction those hits should unlock is not yet realized, because the cached tensors do not yet reach the attention kernel. Closing that one gap is what converts a correct accounting of savings into observed savings.

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